# **Difference Between Von Neumann and Harvard Architecture**

Von Neumann and Harvard architecture are known to be the two basic models on which computer systems are based. The significant difference between Von Neumann and Harvard architecture arises according to the way the CPU is separated from the memory. In both these architecture, two different ways are used by which memory is accessed by the CPU.

The Von Neumann architecture is also known as **Princeton architecture** was proposed by John Von Neumann in the year **1945** and it is an architecture where the data and programs are subjected to shared memory i.e., are stored in the same memory block. As against, Harvard architecture is such an approach where data and instructions do not share the same memory i.e., are present in different memory blocks.

It is generally said that Harvard was proposed to deal with the limitation of Von Neumann architecture.

## Content: Von Neumann Vs Harvard Architecture

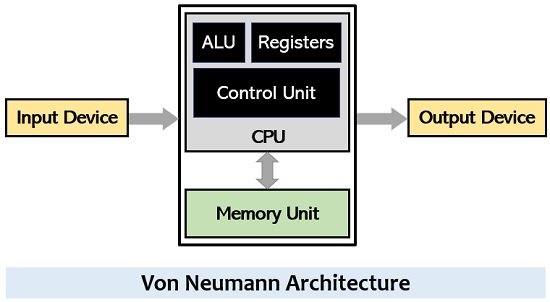
1. [Comparison Chart](https://circuitglobe.com/difference-between-von-neumann-and-harvard-architecture.html" \l "ComparisonChart)
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### **Comparison chart**

| **Basis for Comparison** | **Von Neumann Architecture** | **Harvard Architecture** |
| --- | --- | --- |
| Basic | Data and instructions reside within a single memory unit. | Data and instruction are provided 2 different memory units. |
| Based on | Stored program computer concept | Harvard Mark I relay based model |
| Memory system | Single | Dual |
| Required space | Less | Comparatively more |
| Set of address/ data bus | One | Two |
| Development cost | Low | Comparatively more |
| Efficiency | Less | More |
| Execution speed | Slow | Comparatively fast |
| Operation | Simple | Complex |
| Performance offered | Low | Comparatively high |
| Clock cycle | Single instruction is executed in minimum two clock cycles. | Single instruction is executed in one clock cycle. |
| Feature | Data transfer and instruction fetching do not occur simultaneously. | Data transfer and instruction fetch take place at the same time. |
| Space utilization | Good | Not so good |
| Applications | PCs, workstations, notebooks, etc. | Microcontrollers, digital signal processing, etc. |

### **Definition of Von Neumann Architecture**

A computer architecture that uses a single memory unit within which both data and instructions get stored is known as Von Neumann architecture. The figure below represents the architectural representation of the Von Neumann Model:

[](https://circuitglobe.com/wp-content/uploads/2021/06/Von-Neumann-Architecture.jpg)

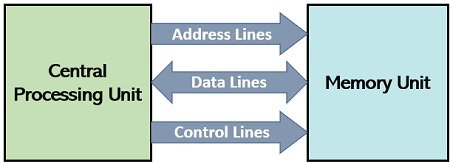
There are three major components that constitute this architecture:

* CPU
* Memory
* I/O interface

The central processing unit is composed of the control unit, arithmetic and logic unit, and registers. The control unit is responsible for generating control signals based on the order of executing the instructions. This means that the control signals are provided to the various components within the architecture for the proper flow of information. The ALU is responsible for executing the mathematical operations. While the registers are responsible for temporarily storing data and instructions.

The memory unit also serves as a crucial part of the overall system as it stores both data as well as codes. A computer’s memory is mainly classified as RAM and ROM. RAM is the temporary storage unit that stores data along with general-purpose instructions. While ROM is a permanent type of memory that holds the instructions responsible for booting up the system.

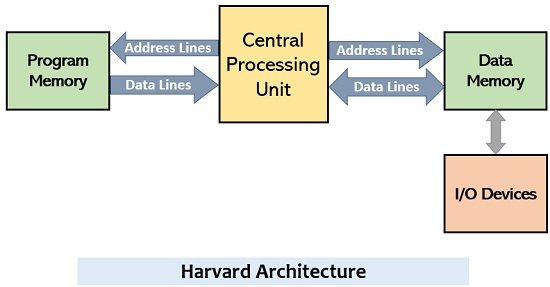
Like we have said that in this architecture, data and instructions both reside in a single memory unit hence a single set of buses is used by the CPU to access the memory.

[](https://circuitglobe.com/wp-content/uploads/2021/06/data-transfer-between-CPU-and-memory.jpg)

After the execution of the program, data gets stored in memory from where it is provided to output device.

### **Definition of Harvard Architecture**

A computer architecture where the memory unit is divided into two parts for individually storing data and instructions is known as Harvard architecture. This means, unlike Von Neumann architecture, here data memory and instruction memory is in separate format. The figure below shows Harvard Model:

[](https://circuitglobe.com/wp-content/uploads/2021/06/Harvard-Architecture.jpg)

Here in this architecture, the CPU operates in a somewhat similar manner as in Von Neumann architecture. But as here two separate memory units are used thus separates buses are used for data transferring and instruction fetching. Thus, execution speed is very much faster than Von Neumann architecture.

In this approach, efficient resource utilization occurs as instructions bits are sometimes more than the data bits thereby permitting different cell sizes. Also, the use of separate memories for both data and instructions helps in the minimization of execution time. However, in the Harvard model, the central processing unit present must be more efficient so that it can handle two sets of buses and allows simultaneous data transfer and instruction fetching.

## Key Differences Between Von Neumann and Harvard Architecture

1. The **key factor** of differentiation between Von Neumann and Harvard architecture is that in Von Neumann architecture a single memory containing both data and instructions is accessed by the CPU. On the contrary, in Harvard architecture, individual memory units are present for data and instructions that are accessed by the processor.
2. The presence of a single memory unit makes the system composed of Von Neumann architecture quite **compact** in comparison to the system with Harvard architecture as it has more than one memory thus is bulky.
3. In Princeton architecture, a common bus is used for data and instructions. While in Harvard architecture separate set of buses is used for transferring the data and instruction fetching as two separate memory units exist here.
4. The **cost to develop** a system with Von Neumann architecture is comparatively less than the developing cost of a system with Harvard architecture.
5. One of the important **features** of Harvard architecture is that it offers data transfer and instruction fetching from the memory at the same time because it comprises two sets of buses for the operation to take place. As against, this is not the case with Princeton architecture as the single bus is used for both data transfer and instruction fetching hence the two tasks cannot take place simultaneously.
6. The Von Neumann architecture needs less **space** as it has a single memory unit but the Harvard architecture comparatively takes more space due to multiple memory units.
7. Von Neumann architecture exhibits a slower **execution speed** because it does not permit simultaneous processing while the execution speed offered by Harvard architecture is more.
8. Though the speed of executing operations is less in the case of Von Neumann, here the **implementation** is quite simple however Harvard architecture offers comparatively complex operation.
9. The hardware requirements of the two architectures are also different. In Von Neumann architecture a single memory is accessed thus **hardware requirement** is low. On the contrary, in Harvard, two memory units are accessed thus hardware requirements will obviously be high.
10. The **utilization of space** within the memory is a major issue in the Harvard model as here the data and instructions are stored separately thus, even if some space is left in data memory, no instructions can utilize that space. However, the space utilization factor is comparatively better in the Von Neumann model because both data and instructions are stored in the same memory unit.
11. In Von Neumann architecture, an instruction execution takes place using two **clock cycles**. But with proper pipelining, in a single clock cycle, a single instruction can get executed in Harvard architecture.

### **Conclusion**

Thus, from the above discussion, it can be concluded that the Harvard architecture is somewhat an improvisation in Von Neumann architecture by offering a comparatively better design thereby providing simultaneous execution. However, various modern systems do not offer physical separation between data and program memory thus, is said that these are based on Von Neumann architecture.